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# DESIGN AND IMPLEMENTATION OF LOW POWER, AREA AND HIGH PERFORMANCE 4 BIT SEQUENCE DIGITAL COUNTER

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**Abstract-**The goals of the low power VLSI circuit are to decrease the system's energy footprint and power consumption while increasing the battery life and performance. The scaling architecture, often known as a counter, modifies the values of an operator depending on its previous state. It's possible that the counting procedure might provide time and frequency data. Clock power dissipation during standby is the primary reason of the excessive power consumption of scaling circuits. About one-third of a counter's total power is used up by the clock signal. In order to save energy, this research minimizes the number of switches used. The low power consumption of the counter is the result of work done to reduce the stress on the flip-flops. Combining TSPCL with SVL (Self-Controllable Voltage Level) is a viable option for accomplishing this goal. TSPCL can execute the Flip-Flop operation rapidly while using minimal power. The SVL technique is simpler since it requires fewer transistors and hence consumes less energy due to leakage current. The new model saves 27% more energy than the previous one. The proposed method locates feasible functions for cutting-edge, low-power devices.

**Keywords-** TSPCL, SVL, flip-flops.

## I. INTRODCUTION

In logic circuits, a Flip-Flop is used to generate a 0 or a 1. Its primary use is archival storage. The flip-flop is unparalleled when it comes to sequential storage. In a scalable circuit, the number of repetitions of a process or event may be counted by inputting a clock signal. It counts the number of pulses received from the input line. Maintaining a reliable clock that uses minimal power is essential. This results in reduced power consumption by the circuit. Both synchronous and asynchronous counters are employed in Complementary Metal-Oxide Semiconductor Very Large Scale Integration. The output of one Flip Flop (FF) may serve as the clock input for the next FF in an asynchronous counter, but

this is not possible in a simultaneous counter. The propagation time may be decreased by using a unique single-edge triggered D FF, although this kind of FF is not appropriate for higher operating frequencies. Multiple binary inputs may have their output compressed using a low-power scaling circuit that uses priority encoding. With a quasi-synchronous layout, energy is dissipated at a faster pace. Scaling circuit for a pseudo clock. These methods may produce effective layouts, but their scalable blueprints are prohibitively large. For low-power scaling, bi-stable storage components are often used in designs.

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## II. EXISTING METHOD

### A. D FLIP FLOP WITH MODIFIED TSPCL

To make the flip-flop, the True Single Phase Clock technique is employed. The basic goal of TSPCL [1] is to carry out the necessary Flip-Flop operation at maximum speed while using as few transistors as possible. The D Flip-Flop seen in Figure 1 was created using [2] TSPCL. The N2 transistor is active when  $D = 0$  and  $CLK = LOW$ , which in turn activates the P1 and P2 transistors. Since P3 does something useful, it gives you back a 1 (which becomes a 0 when you flip it). D has its input gradually reversed while maintaining the same output.

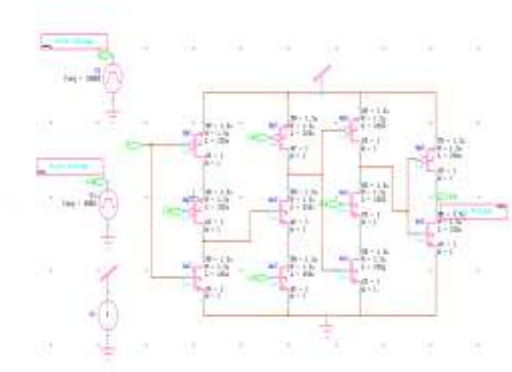


Figure 1: Schematic of TSPCL D flip flop



Figure 2: Simulation of TSPCL D flip flop

### B. UPPER SVL:

There are three transistors shown in the following diagram; two NMOS and one PMOS. [3]. A PMOS and two NMOS are connected in series to create the top-tier SVL. Both the input clock bar and one of the power supply's NMOS gates are in the PMOS state. Setting  $clk$  to 1 activates PMOS. The supply voltage is thus conducted via the PMOS. At  $t=0$ , the two NMOS devices start conducting and establishing a ground connection. It is possible to limit leakage power by connecting the NMOS in series while the circuit is turned off. The superior vena cava lobule is.

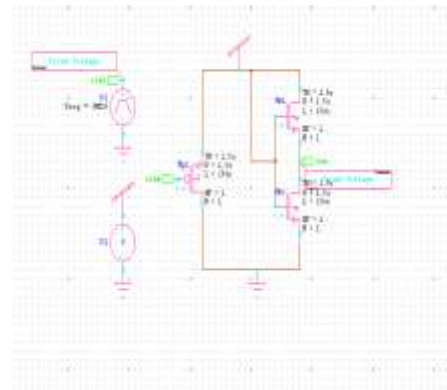


Figure 3: Schematic of Upper SVL

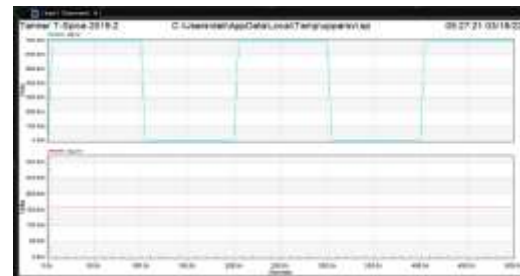


Figure 4: Simulation of Upper SVL

### C. LOWER SVL

The image above depicts three different transistors: two PMOS and one NMOS. Two PMOS and one

NMOS make up the bottom SVL. The PMOS gates receive the input clock and the NMOS gate is at ground. If  $calk$  is 1, then NMOS is not enabled. When a PMOS is connected to a grounding source, it begins to conduct electricity. Setting  $calk$  to 0 activates supply voltage 1. When the device is inactive, the leakage current [2] may be minimized by adjusting the bias. The SVL is decreased as seen in Fig. 3. The most typical implementation of the CMOS D FF circuit [10]. In CMOS technology, leakage power is crucial. It is possible to reduce the supply voltage when the circuit is switched off, which helps save power and prolongs the battery's life. The SVL approach is used in the CMOS D FF circuit to lower power consumption and signal noise [7]. Dynamic power consumption is reduced in the new design as a direct consequence of using fewer transistors.

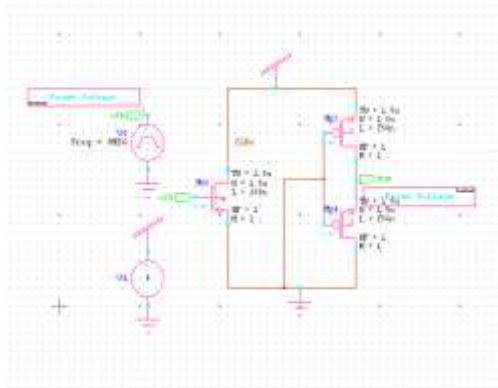


Figure 5: Schematic of Lower SVL

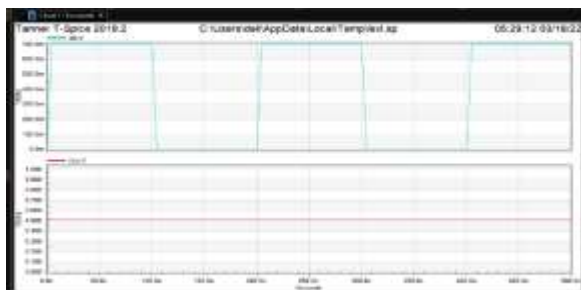


Figure 6: Simulation of Lower SVL

#### D. D FLIP FLOP WITH MODIFIED SVL:

There are a total of 15 parts in the above diagram, seven PMOS transistors and eight NMOS transistors. [8]. N1 and N2 of the D flip flop are disabled [9] when the SVL is changed. The D Flip-Flop can't function without power and ground. There are two static (P2) and three dynamic (N1) states in this situation. While P1 is offline, P2 is operating normally. There is an "open" setting on both the P1 and N3 switches. The supply voltage for N1 and N2 to act as pull-up networks must be between  $V_{DD}$  and  $V_T$ . Reducing static power by connecting NMOS transistors in series [10]. In lieu of GND, P2 and P3 create a pull-down network with a little positive voltage. By putting NMOS transistors in series, supply voltage and leakage current may be lowered during standby. Because of its link to the input voltage and current, leakage power is notoriously difficult to cut down on. As a bonus, this layout significantly reduces the circuit's dynamic power consumption without sacrificing performance. Figure 4 depicts the D FF's new and enhanced SVL configuration.

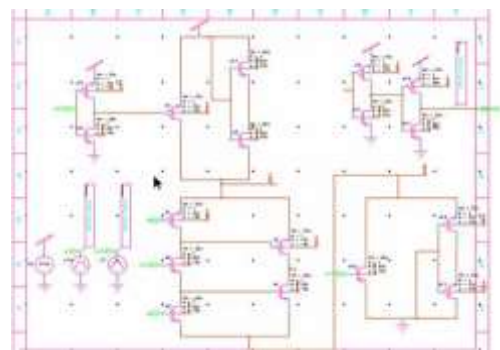


Figure 7: Schematic of Modified D Flip flop using SVL

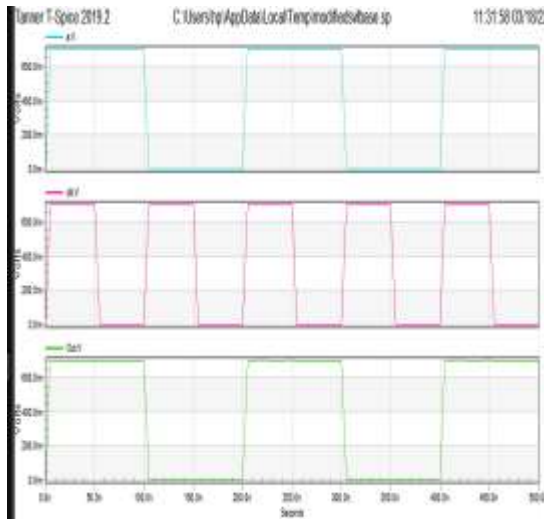


Figure 8: Simulation of Modified D Flip flop using SVL

### E. DESIGN OF D FLIP- FLOP USING STATIC CMOS

Dynamic mode static CMOS transistors were used to construct the aforementioned D flip flop utilizing the aforementioned block. Since a statically built D flip flop needs 20 transistors,[3] switching to a dynamic approach will lower the number of transistors needed. As a result, cutting down on the space required for semiconductors is crucial. This design uses just around 5 transistors, as opposed to the nearly 20 transistors needed to create a D Flip flop using NAND [7] gates. When applied to such layout, the suggested technique yields efficiencies of about 40%. In CMOS digital circuitry, there are three potential causes of power loss. First, the signal transistor itself drains current, then leakage drains current, and finally the short drains current from the power supply to ground. When the threshold voltage and gate oxide thickness on the channel length are decreased, significant leakage current dominates the power dissipation of CMOS devices. The D flip-flop design presented uses a total of five transistors (three NMOS and two PMOS; see Figure 5.1 for details).

### III. PROPOSED 4 BIT COUNTER DESIGN

#### A. D FLIP FLOP USING 5 TRANSISTORS

Multi-threshold complementary metal-oxide semiconductors and D flip-flops are rolled into one convenient term. Figure 5.1 depicts a positive edge that triggers a 5 Transistor D latch. Transistors N1, N2, and P2 will be enabled, while Transistors P1 and N3 [4] will be inhibited, if both Clock and input are high. The rate of output is rising. In a single clock cycle, the input value is converted to the required output. Figure 3 shows a schematic for a very high-quality, five-transistor D-flip-flop. The clock is high (transistors P2 and N2 are "off"), the input is low (transistors P1 and N1 are "on"), and the N3 transistor is "on" (because of the low output) when the D flip-flop's output is low. When the output is in the high state (high impedance) and the clock input is also high, the P1 transistor is "off," the N1, N2, and P2 transistors are "on," and the N3 transistor is "off." In the event that the clock input is low, the output [5] will also be low, turning "on" the P1 transistor and "off" the N1, N2, P2, and N3 transistors. After the initial layout was finalized, the circuit was put through its paces with the help of the Tanner EDA tool (see Fig. 1). The S-Edit circuit is simulated when it is constructed. If the inputs are same, the results should be identical as well.

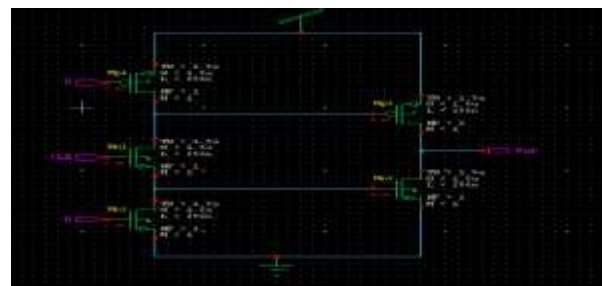


Figure 9: Schematic of D Flip flop using 5 Transistors



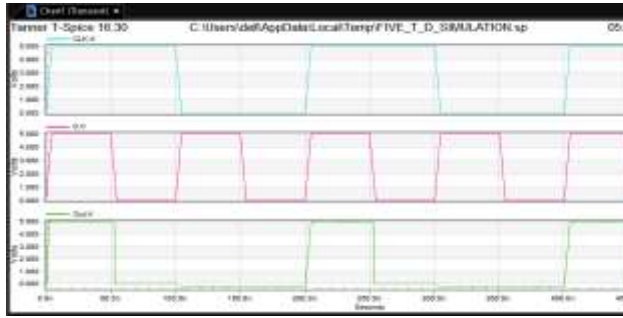


Figure 10:..Simulation of D Flip flop using 5 Transistors

A 5-transistor D flip flop, shown schematically below, generates a 1 when CLK is high and a 0 when CLK is low.

### B. Design of XOR Gate Using Pass Transistor

The following diagram depicts an XOR gate implemented using pass transistor logic; the input, which would normally be connected to the transistor's gate terminal,[6] is shown instead connected to the element's source and drain.

The above diagram shows a circuit that uses two transistors. The outputs of two pass transistors are linked at the output node when one pass transistor is used to propagate the ABAR signal with the B signal as its gate input and another pass transistor is used to propagate the A signal with the BBAR signal as its gate input.

To build an XOR gate employing PASS transistors, this design was implemented. Passing transistors help decrease the need for the 12 transistors needed for a static CMOS architecture.[7] Consequently, we'll be able to shrink the semiconductor in size by using pass transistors. A pair of CMOS inverters and a pair of NMOS transistors are required to construct an XOR gate. Because it uses just two transistors, the aforementioned architecture significantly reduces both power consumption and the size of your device.

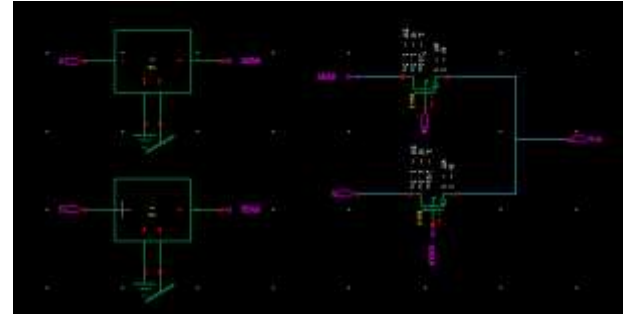


Figure 11: Schematic of XOR gate using 6 Transistors

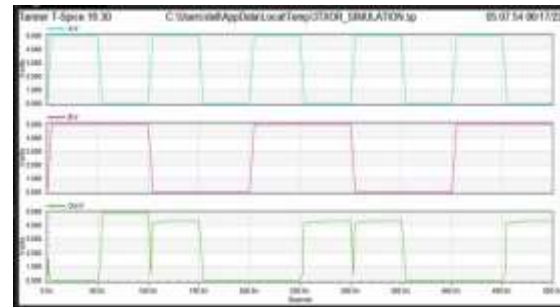


Figure 12: Simulation of XOR gate using 6 Transistors

If the logic levels of its two inputs, A and B, are the same, the output of the simulated XOR gate [8] is zero, and if they are different, the output is one (as seen in the image above).

### C. PROPOSED COUNTER DESIGN

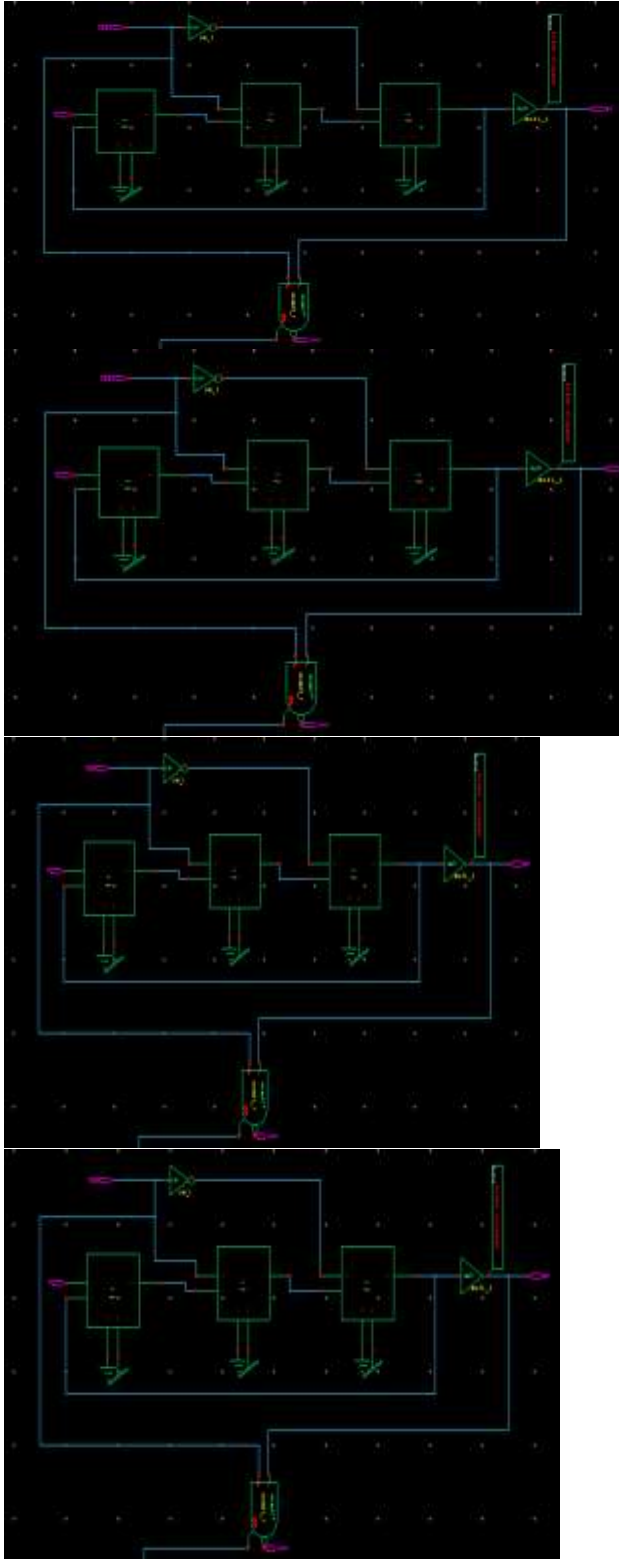


Figure 14: Schematic of Proposed 4 BIT Counter with modified XOR-D Flip-Flop

The counter was built using a single XOR gate,[9] two D flip flops, a master/slave inverter, and a buffer. With each passing second, the outputs of this 4-bit synchronous counter cycle through the values 0 to 15. There are many names for this kind of counter. One of them is 4-bit Synchronous up Counter.

To sum up, below are the most important aspects of Synchronous Counters:

- Toggle or D-type flip-flops may be used to construct synchronous counters.
- Since the clock inputs of the flip-flops in a synchronous counter are all locked to the same signal, their implementation is simpler than that of an asynchronous counter.
- In reaction to this shared clock pulse, all output states shift at the same time.
- When all clock inputs are connected in series, there is no time wasted due to signal propagation. Because the clock is sent to all of the flip-flops simultaneously, synchronous counters are also known as parallel counters. Internally, a memory circuit records the most recent counter reading.
- Due to the employment of logic gates to regulate the counting sequence, synchronous counters may be more efficient than their asynchronous equivalents.

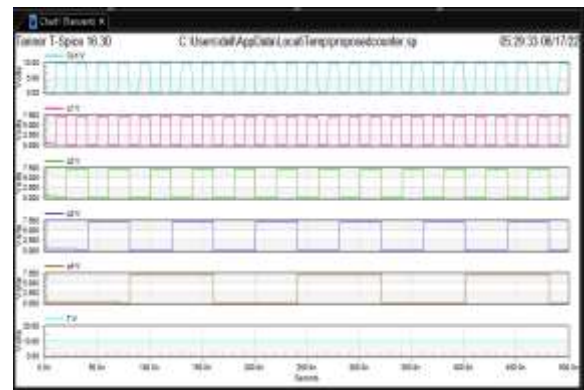


Figure 15: Simulation of Proposed 4 BIT Counter with modified XOR-D Flip-Flop

On the falling edge of the sixth CLK signal, the FF-  
An output will again go low and then high. Logic  
gates A1 and A2 will be turned on since the sum of  
QCQBQA's outputs is 10. On the clock's falling edge,  
the sixth CLK signal changes the state of flip-flop A  
from one to zero. The high input causes the output of  
flip-flop B to alternate between 0 and 1. Here, 110  
stands in for the letters QCQBQA. On the ninth CLK  
signal's falling edge, all FF outputs, including  
QCQBQA, will be reset to 000, and the procedure  
[10] will start again. In a circuit including  
synchronous counters, it is crucial that all FFs be  
reset at the same time. Each flip-flop in the circuit  
causes a delay, and that delay adds up to the total  
time required to initialize the counter. Therefore, a  
high-frequency CLK signal may be used to manage  
this counter.

Comparison of results between existing & proposed  
design:

**Table 1: comparisons of Result**

S.no	Parameters	Existing Technology -250nm	Proposed technology -16nm
1	Area	184 Transistors	76- Transistors
2	Power	4.68 Watts	0.01102 watts
3	Delay	10.2946n	90Ps

The table above compares the existing design process  
[11] with the suggested design strategy. To ensure  
that our novel approach has lower power  
consumption than the norm, we employed the

#### IV. CONCLUSION

T-Shoe-Shaped Sandal The current counter is built  
using T Flip flips, USVL, and LSVL techniques.  
Clock gating raises both power and space  
requirements, however the suggested method  
produces a simultaneous counter with reduced power  
consumption. In this setup, the Flip-Flops are  
required for the clock to switch time zones. The  
complexity issue with the circuit is therefore  
resolved. By reducing the power output of leakage  
current and getting rid of unnecessary transistors,  
pass transistor technology simplifies circuits. The  
redesigned layout reduces energy use by 46.8  
percent. The proposed method locates feasible  
functions for cutting-edge, low-power devices.

#### A. FUTURE SCOPE

Since the suggested strategy allows us to utilize fewer  
transistors overall, it is beneficial in situations when minimizing  
power consumption is of the highest significance.

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