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PMOS BIASEDSENSEAMPLIFER DESIGN WITH LOW POWER AND HIGH PERFORMANCE

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Abstract:

Sense amplifiers plays a significant roleintermsofitsrecital,functionalityandreliability of the memory circuits. In this papertwonewcircuitshavebeenproposed.Theproposed circuit is PMOS biased sense amplifier,which provides very high output impedance andhas reduced sense delay and power dissipation.Assuch,theproposedcircuitperformstheidenticaloperationsasthatofconventionalcircuits but with the reduced the sense delay andpowerconsumption

The growing gap between the processorand embedded memory speed is a major setbackin the overall performance of electronic systems.Since the sense amplifier (SA) forms an integralpartofthereadcircuitryinbothvolatilememories,suchasSRAM,andnon-volatilememories(NVMs),suchasFLASH,itsperformancehasasignificanteffectontheoverall performance of memory. Access time,offset,power andarea are the four importantperformance metrics of SA. The memory accesstime and input-offset of SA greatly affect thespeedoftheentirememoryandthereforetopatch up the gap between processor and memoryspeed, the SA is required to be fast and efficient.As one SA is employed for each bitline in thememory array, it is required to be compact insize and should have low power consumption.Furthermorescalingintechnologymakesitdifficulttocontrolthefabricationprocessleadingtovariationinprocessparameterscausing unpredictability in the performance ofSAs. Therefore, it is very important to keep thisaspect in mind while designing and estimatingtheperformance metricsoftheSA

This thesis includes the study of variousconventional SA designs in detail so as to have abetterunderstandingofabasicSAanditsoperationandthushelpinginunderstandingwhatproblemsarefacedbydesignersinimplementingthe SA designs and how these problems can betackled.InadditiontotheconventionalSAanalysis, new sense amplifier designs have beenproposedforbothcurrentsensinginFLASH memory and voltage sensing in SRAM. Keepingthevariationinprocessparametersduetoscaling inmind,these proposeddesignshavebeen optimized in terms of access time, offset,powerandarea.

Keywords: Sense Amplifier, High Performance,PMOSBiased

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1.

2. INTRODUCTION

In any digital logic design memories arethemostimportantblocksinDSP,microprocessors,microcontrollers,andcomputers. Audio players, digital cameras storesthe data in the form of images, audio, video,speechinaflashmemoryshouldhavelesspowerwiththedisplayofmemorycapacityperformance on high side on a single chip. Lowsensingdelayandincreasedhighercapacities are required for improved quality of stored data.Inordertoaccomplishthetoweringrateofstaging

, sense amplifiersare customarily appliedto amplify the very small voltage difference onthe bit lines at congruous sense timings . If thesense amplifiers enable signal is asserted early,the SAcannotamplifytheminuscule voltagedifference accurately.Theoverheadofaccesstime and power consumption is incremented iftheSAEisassertedtardy.Consequently,theoptimum timing for SAE is critical for a high-speed and low-power SRAM.The memory cellneed to have a mechanism in order to store datapermanently and alter its contents electrically ina non-destructiveway.The solution is to alterthe threshold voltage of the all so that differentthreshold values mayrepresent differentstatesof the memory. The two basic states of a flashmemory cell are called erased and programmedstates.Anerasedcellissignifiedbyalowthreshold value whereas a high threshold valuesignifiesaprogrammedcell.Equation1.1expressestherelationbetweenthethresholdvoltage of MOS with the charge stored on thefloatinggate.

WhereKdenotesaconstantwhichdependsongateandsubstratematerial,channel dopingando_{xide}thickness.C_{ox}denotesthegate oxide thickness and Q is the charge trappedinto the oxide layer. From the equation it is clearthat the parameter which can be kept in controltoalterthresholdofthedeviceisQwhichdenotes the charge trapped in the oxide layer.There are charge injection techniques availabletomovechargesinandoutoftheoxide.Anormal MOS device cannot be used to retain thecharges into its oxide thus the device has beenmodified. A floating gate (FG) device is DMA test mode is used for the used forthis purpose. FG transistors have the capabilitytoretainchargeintheirfloatinggateforanextended period even after the power supply isturnedoff.

DuringtheWrite/Programoperation,thecontrolgateanddrainarebiasedathighvoltage of 12V for the gate and 5 V for the drain(thevoltagesusedforbiasingareusedasconventionandmayvaryfordifferentmanufacturers), but the source is kept grounded.Underthesecircumstances,averystrongelectric field develops which lets the electronspass from the channel to the floating gate. Theseelectrons overcomethepotentialbarrierposedby the oxide layer and this mechanism is calledHotElectronsInjection .

Due to the presence of a high voltage onthe drain node, the electrons flowing from thesourcetothedraingainenergyduetotheorthogonal electric field. Due to the presence ofhighelectricfields,electronenergystartstoincreaseandthuselectronsareheated,someelectrons gain energy high enough to overcomethebarrierbetweentheoxidelayerandthesiliconconductionband.Thesehotelectronsneedtoovercomethebarrierintherightdirection so as to be collected inside the floatinggate. The electrons trapped inside the floatinggate causing the V_{TH} ofthe flash memory cellto rise. Thus, when a Read operation occurs, thecell appears to be in the switched off state or islogicprogrammed‘0’,sinceitisunabletoconductcurrentduetoitshighV_{TH}.Thuswriting data in a memory cell brings the cellfrom an erased state, which is typically called alogicstate‘1’,toalogicstate‘0’orprogrammedstate.Thetimerequiredforthisprocessistypicallyinthe rangeofmicroseconds.

purposeofconnectingthecellterminalsdirectlytothe

externalInput/outputpads.Thishelpsincharac terization of the memory, the matrix andthe reference cells in particular. It is a difficulttasktofiltertheinterferenceofthemem oryarray. Many incorrect outputs can be obtained tothe faults in circuitry if any. For example, if thevoltages are applied in the wrong way or if thereis a presence of any voltage spikes or glitches.The possibility of analyzing each and every cellisthereforeavaluableopportunity.Evenas inglecellcanbeanalyzedwiththehelpofDMA thus proving to be a major test mode. TheDMA test mode setup is shown in Fig. 7. It canbe observed from Fig. 7. that in DMA the senseamplifier and the output latch are bypassed suchthatthedrainnodeofthecellisdirectlycon nectedtotheexternalI/Opadwhichisfurtherco nnectedtotheexternalsupply.Thesupply voltage of this external supply is equal tothat on the drain in case of a read operation.Also, the gate voltage supplied to selected cellsin DMA mode is supplied through an externalpin.Thissetupenablesthemanufactur erto measure cell current, transconductance and V_{TH} ofcellsundervaryingcondition.

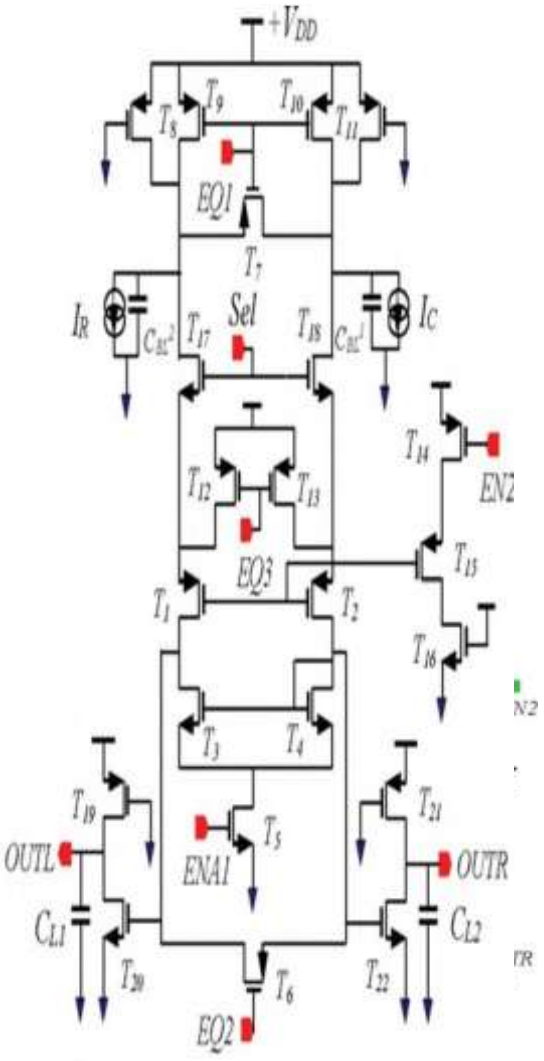
OperatinginDMAmodesoastomeasur ethecellcurrentatdifferentbiasvoltagesis a tedious job. Therefore to increase the speedofthisprocedure,FastDMAorFDMAwa sintroduced. FDMA mode is similar to the readmode but in FDMA mode a constant referencecurrentismaintainedandthecellcurre ntiscomparedwithitwiththehelpofasenseampl ifier.Thereferencecurrentcouldbegeneratedin ternallyorcouldbegeneratedexternally with the help of the DMA pin. Thegate voltage could be controlled by an externalI/O pad similar to DMA mode. By varying thiscurrent and gate voltage the cell characteristicsare plot. FDMA has an advantage over DMAbeingfasterduetothereadoperation.

i.LITERATURESURVEY

It is organizedintofivesections.discusses about few conventional SAdesigns and includes their detailed study. Firstlyintroduces a high speed low offset cross coupledlatchtypecurrentsenseamplifierforNVMappl ications and the Flash memory in particular.Thedesignanditsworkinghasbeenexplaine dindetail,thedesignhasbeensimulatedananalyzedbyi ncorporating V_{TH} variationsandtheoutputshavebeen presented.Section4discusses about the low offset high speed crosscoupled latch type SA for SRAMapplications,in which offset and sensing delay lowing havebeen achieved using body biasing techniques. Inthis section, the design has been explained indetail, it has been simulatedandanalyzedbyincorporatingMCVTHvari ationsof10mVinallthedevices.Theoutputsfor thissenseamplifierdesignforSRAMhavebeenpresent ed.

ii.EXISTINGSYSTEM

Comparison of differentcurrentmodesenseamplifiersispresented. Inthose circuits, we considered PMOS biased senseamplifiercircuitsasareferencescircuitforpropos ed method by,making some modificationsin it.In this circuit, there exists two differentialamplifier



circuits with current mirrors which ithastobe modifiedin theproposedcircuit

iii.PROPOSEDSYSTEM

Afastaccesstimeandlowpowerdissipation are achieved with newly developedcircuits of sense amplifier for low voltage supply.In the proposed circuit Here minimizing the mirrortransistor so we can have low power dissipationwithhighperformanceandlesssensedelay.

Fig.1 Existing Sense Amplifier circuit

Fig 2: Proposed Sense Amplifier circuit

CIRCUIT DIAGRAM

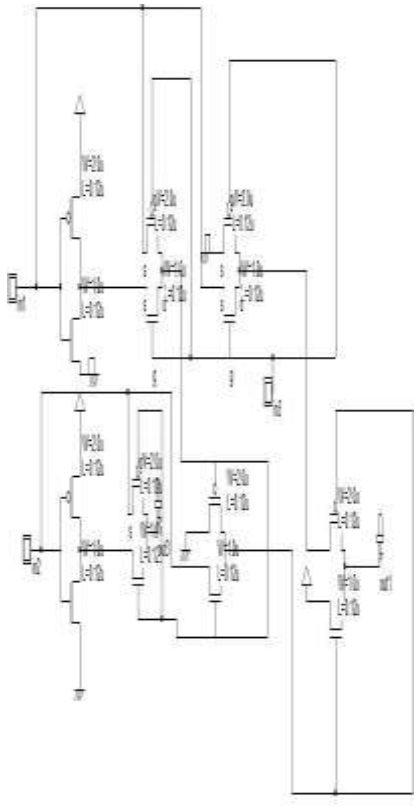


Fig 3:PMOSSenseAmplifier

2.WORKINGPRINCIPLE

It has three inputs and two outputs withfive stages. It has Inversion amplifier means itinverse theinputandperformthecircuitandfinaloutput isgivenasinverseoutputforavoidingofconfusion.Stageshelpforgettinghigh performance with low power dissipation.ItisthecombinationofPMOSandNMOStransistorswhichperformsPMOSasLeadingandNMOSasLagging.

Thecircuitconsistsof7CMOStransistors which is the combination of PMOSandNMOS.Whenweprovideinputswegetdifferent type of outputs (don't care condition)accordingtoinputsprovided.Wheninputsare Low,LEDisinOFFstate.WheninputsareHigh,LEDisinONstate.

3.SOFTWARE

DSCHMicrowindisbasicallydigitalschematiccircuitdesigningsoftware.Thisismicrowind simulation software which allows theusers to simulate and design integrated circuit atphysical description level. This is user friendlycircuit simulation software and it supported byhugesymbollibraries.Microwindunifiesschematic entry, pattern based simulator, SPICEextractionofschematic,Verilogextractor,layoutcompilation,onlayoutmixed-signalcircuit simulation. Microwind software helps todesign various types of logic gates: AND, OR,NOR, NAND, XOR and many advanced designincludedwithhalfadder, fulladder etc.

The DSCH program is a logic editor andsimulator.DSCHisusedtovalidatethearchitectureofthelogiccircuitbeforethemicroelectronicsdesignisstarted.DSCHprovidesauserfriendlyenvironmentforhierarchicallogicdesign,andfastsimulationwith delay analysis which allows the design andvalidation of complex logic structures. DSCHalso features the symbols, models and assemblysupportfor8051andPIC16F84controllers.Designerscancreatelogiccircuitsforinterfacingwiththesecontrollersandverifysoftwareprograms usingDSCH.

In the first part of this article we willdiscuss thebasic logiccircuit.Inthenext partwewillmovetoadvanceddesign.Let'sconside

r 2-input AND gate. Though most of youknowANDgateoperationbutthisarticle istotally introductory level discussion.there is noinput signal so that the output is zero. A HIGHoutput results only if all the inputs to the ANDgate are HIGH If none or not, all inputs to theAND gate are HIGH, a LOW output result.Thefunctioncanbeextendedtoanynumberofinputs.

- User-friendlyenvironmentforrapiddesignoflogiccircuits.
- Supportshierarchicallogicdesign.
- Addedatoolonfaultanalysisatthegatelevelofdigital.Faults:Stuck-at-1,stuck-at-0.Thetechniqueallows injectionofsinglestuck-atfaultatthenodesofthecircuit.
- ImprovedinterfacebetweenDSCHandWinspice.
- Handlesboth conventional pattern-basedlogicsimulationandintuitiveonscreenmouse-drivensimulation.
- Built-inextractorwhichgeneratesaSPICEnetlistfromtheschematicdiagram(Compatible with PSPICETMandWinSpiceTM).
- GeneratesaVERILOG description oftheschematicforlayoutconversion.

4.ADVANTAGES,DISADVANTAGES& APPLICATIONS

- Thisproposedsenseamplifierwhichisimplemented in PMOS process can work atvoltageas lowas 1V.
- Astheproposed SAworksat3.3V,thisdesignhas14%and63% powerdelayproductImprovementovertheadvancedcurrentlatchSAandconventionalsenseamplifier,respectively.
- Areaisreducedbyminimizingoftransistors.Sensedelayisalsoreduced

Disadvantages:

- Due to process variations, current mismatchintheevaluationbranchesofthesenseamplifiercircuit,resultinginoperationalfailures.Sizeofthissenseamplifierarchitectureisla rge.
- The worst power consumption is observedinthistype ofsenseamplifier.

APPLICATION

- **Memoryunits.**
- Microprocessors.
- Microcontrollers.
- Computers**.**

5.RESULT

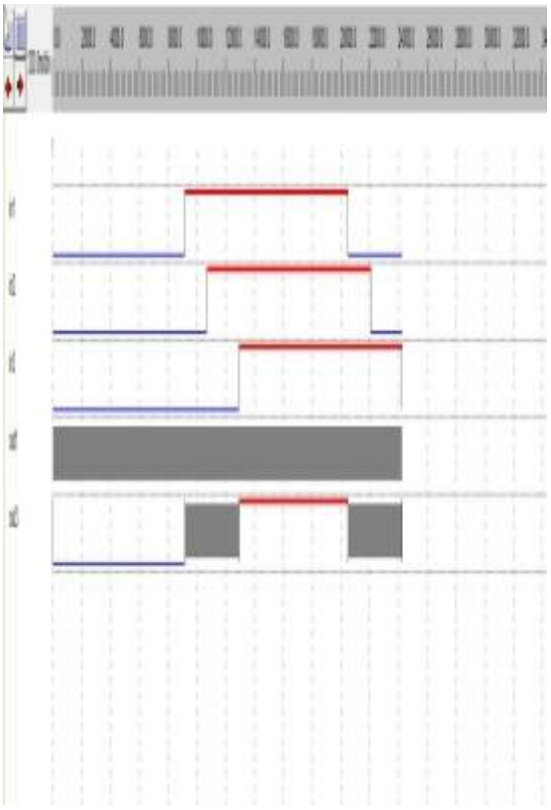


Fig.4: PMOSsenseAmpliferResult.

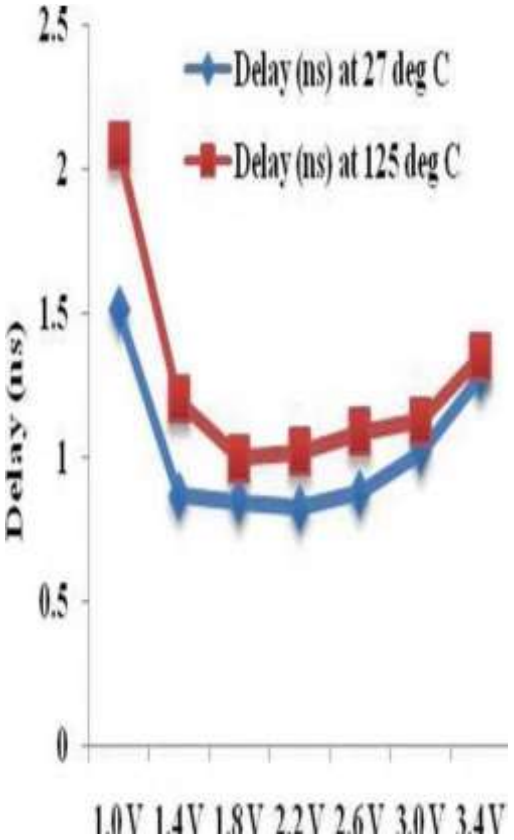


Fig.5: Sensing delay vs Different Voltage.

6..CONCLUSION&FUTURESCOPE

Themainaimofthisprojectistoprovidelowpowerdissipationwithhighperformance and less sense delay in memoryunits.

The proposed SA for NVM shows thatcapacitivecouplingwiththeSAinordertocouplettheloadresultsinlowerpowerdissipationduetoloweringofthecouplingeffectatnodes,alsotheproposedSAsensesoutputfasterataloweroltageoffset.Theproposed SA for SRAM cell shows that whenbody biasing is used in order to strengthen thepositivefeedbackinthecrosscoupledSAtopology,theSAgivesfasterresultsduetoloweringofthresholdvoltagesof pulldowns

FutureScope:

It has been established that SAs form anintegralpartofanymemoryandthusany improvementinthespeed,yieldandoffsetofthe SA will contribute to significantimprovementintheperformanceofmemorycircuitsandsuchimprovementswillhelpbridgeupthegapbetweenprocessorspeedandmemory.Inthefuturemoresuchtopologiescouldbeexploredandthecurrenttopologiescould be analysed for layout work and chip area.Delay can be further reduced byimproving the circuitdesign. Affectofprocessvariations and corner variations on theperformance of the proposed sense amplifiersarenotincluded.Soeffectsofthesevariationsareremovedbyproperdesignofcircuitsandaccuratesimulations.Yieldmeasurementscan bedone.

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