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# DESIGN OF DOUBLE LATCH-MULTIPLEXED OUTPUTS PAR ADIGM BASED POWER GATED DUAL EDGE TRIGGERING FLIPFLOP

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***Abstract*—In this paper we introduce a new Power gated dual edge triggering flip-flop circuit based on double latch-multiplexed outputs paradigm with totally 20 numbers of transistors including 8 numbers of clocked loads. Initially, the single latch L1 is constructed in two stages with minimum numbers of transistors. To construct the double edge triggering flip-flop, the latch L1 is duplicated as latch L2 and these two latches are connected in parallel and act as master slave flip-flop.**

**The sleep transistor technique is one of the power gating methodologies and it is integrated into the new double latched multiplexed master slave flip-flop, for additional power reduction. The sleep transistor technique dramatically reduces the leakage power during the circuit in the mode of sleep. The performance of proposed flip-flop is analyzed by simulating the circuit at 0.12µm CMOS process technology. The proposed flip-flop design offers a power reduction upto 67.89%with considerable speed improvement compared to conventional flip-flops. Also, the performance of proposed design is evaluated by implementing the 4-Bit parallel input serial output shift register. The evaluation indicates that the proposed design is well suited for clocking systems where power dissipation is major concern with considerable delay.**

***Index Terms*—Digital CMOS, double edge triggering, flip-flop, Low power.**

## I. INTRODUCTION

The clocking system, which is constructed by the clock allocation tree and register elements (latches and flip-flop), is one of the major power consuming components in a VLSI system. [1, 2] In the total power dissipation of the system, it accounts for 30% to 60% of the power consumption. Thus, it is essential to reduce the power consumption in both the clock allocation tree and register elements (flip-flops). As a result a reduction of the power consumed by the register elements will have a deep impact on the total power consumption of the clocking system [3]. Low power design methodologies target to reduce the power consumption, thereby obtaining a power efficient register element with high performance.

Leakage currents are important sources of power consumption in modern

CMOS integrated circuits. International Technology Roadmap for Semiconductors states that ″Leakage will become a major industry crisis, threatening the survival of CMOS itself″ [4]. Suppressing sub threshold leakage currents in large scale integrated circuits is essential for achieving low power consumption in modern clocking system design which consists of several logical blocks.

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Logical blocks can operate in two different modes, active mode and standby mode [5.]

Power gating techniques essentially increase the effective resistance of leakage paths by connecting sleep transistors [6] .The PMOS sleep transistor placed between the logical block and power supply VDD is referred as Header switch element. The NMOS sleep transistor placed between the logical block and ground VSS is referred as Footer switch element. The CMOS logic circuit block with real power VDD & real ground VSS is shown in Fig.1. The Fig.2 demonstrates the power and ground gated CMOS logic circuit block with header PMOS and footer NMOS transistor.

If the standard SLEEP transistor technique is directly applied to a register element, the state of the circuit is lost during the SLEEP mode. The design of low-leakage memory circuit with data retention capability is another important factor [7].

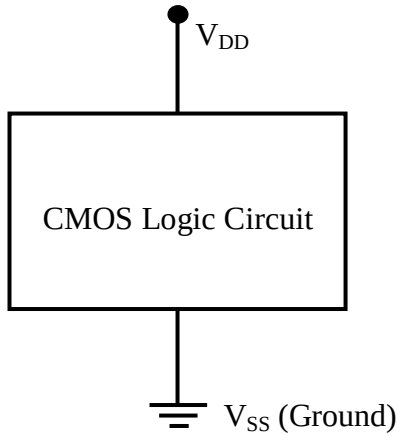


**Fig.1** Basic CMOS Logic circuit with real power VDD & real ground VSS

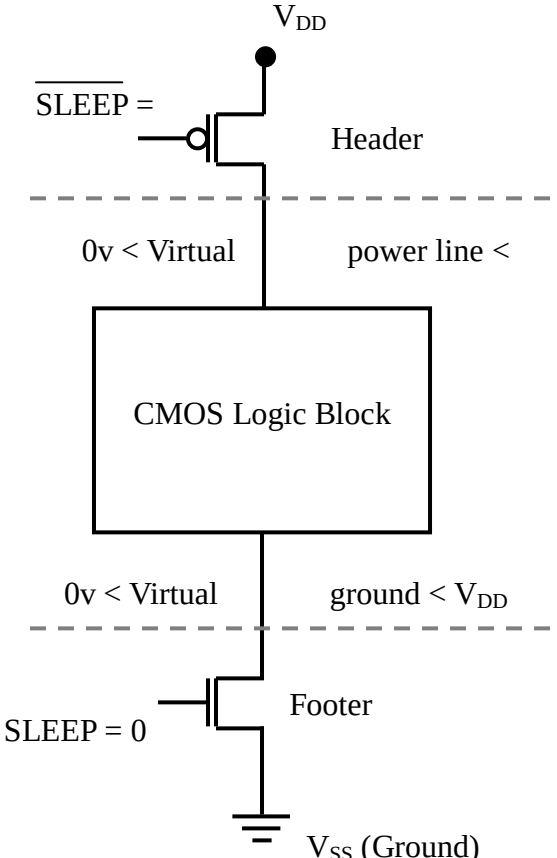


**Fig. 2** Power & ground gated CMOS Logic circuit block

## II. PROPOSED DUAL EDGE TRIGGERING FLIPFLOP

This proposed double Latch-Multiplexed outputs paradigm based power gated dual edge triggering flip-flop [DMO-PGDETFF] for low power clocking system is developed by following double latch-multiplexed outputs paradigm [8]. Initially, the single latch is constructed by two stages. Stage 1 by three transistors P1, N1 & N2 in series and stage 2 by two transistors P2 & N3 in series. The output of first stage is split into two separate outputs (X1, Y1) and given as inputs for second stage. The data input D is given to PMOS transistor P1 and NMOS transistor N2. The CLK signal is given to NMOS transistor N1. It samples the input data D at positive edge of the clock as shown in Fig.3 [9].

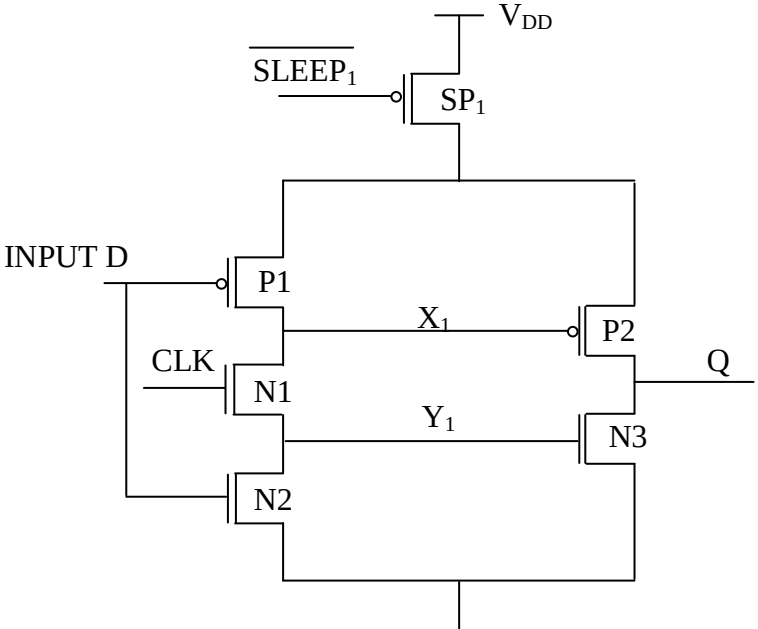

**Fig. 3** Power & ground gated latch L1 with two stages

When positive edge of the CLK arrives (i.e.,) CLK=HIGH (1) and input D=HIGH (1), the transistors N1 and N2 are charged and turned ON and PMOS transistor P1 gets OFF. The ON state NMOS transistors N1 & N2 pulls down the nodes X1 & Y1 to Low value (0). When X is low (X1=0), the P2 transistor is turned ON and at Y is low (Y1=0), the N3 transistor gets turned OFF. The ON state transistor P2 is charged to VDD and results the output Q= HIGH (1).

When CLK=HIGH (1) and input D=LOW (0), the transistors N1 and P1 are charged and turned ON, transistor N2 gets turned OFF. The intermediate nodes X1 & Y1 are charged to supply VDD through the ON state transistors P1, N1 and both X1,Y1 nodes become HIGH(1). Due to X1=HIGH (1) and Y1=HIGH (1), the PMOS transistor P2 is turned OFF and N3 transistor is turned ON. The ON state N3 transistor pulls down the output to low value results output Q=LOW (0).

When Negative edge of the clock arrives CLK=LOW (0), the flip-flop does not samples the input data D. It loads the data D, only at rising edge of the clock CLK = (1).

To construct the double edge triggering flip-flop, the double latch-multiplexed outputs paradigm is followed and illustrated in Fig. 4. The latch L1 is duplicated as latch L2 with first stage P3, N4 & N5 transistors and second stage P4 & N6 transistors. These two latches are connected in parallel and operated as master slave flip-flop, demonstrated in Fig .5.[9].

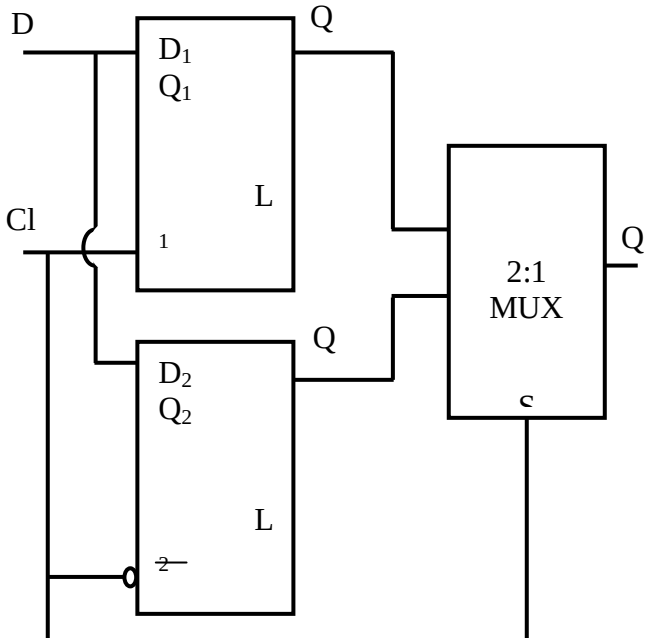


**Fig. 4.** Fundamental double latch-multiplexed outputs paradigm

Master slave flip-flops are not suitable for high speed applications due to its high data to output delay. But they are more power economic, efficient in point of power delay product (PDP) and can be used in low power applications [10].The same input data D is given to P3 & N5 transistors and inverted CLK is given to NMOS transistor N4. The outputs Q1 and Q2 are multiplexed by 2:1 CMOS multiplexer. The CMOS multiplexer is constructed by P5, N7 and P6, N8 transistors and the clock is given as select line input to select the output Q1 or Q2 from latch L1 or latch L2 respectively. The latch L1 samples the data at rising edge of the clock (i.e) CLK=HIGH (1) and L2 samples the data at falling edge of the clock (i.e) CLK=LOW (0). According to the edge arrivals of the CLK, the MUX multiplexes the output and results the output Q at both edges of the CLK. Compared to SETFF, the double edge triggering Flip-flop DETFF requires more transistors to implement. But it halves the clock frequency and leads to power reduction.

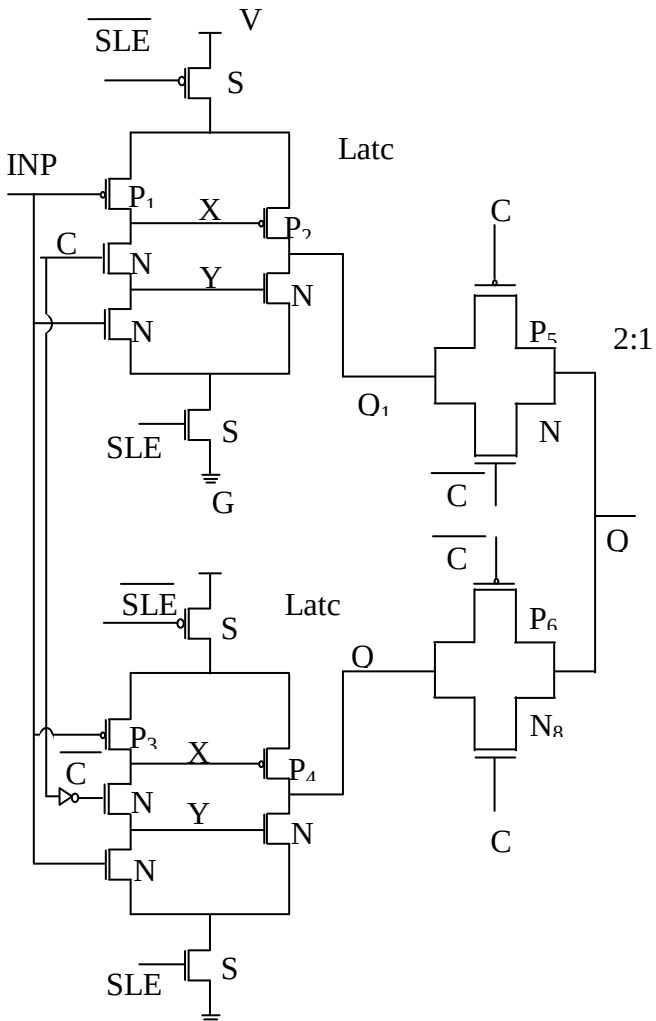

**Fig. 5.** Proposed Double Latch Multiplexed Outputs paradigm based Power Gated Dual Edge Triggering flip-flop [DMO-PGDETFF] includes 8clocked and 12 unclocked transistors (Total 20 numbers of transistors)

The sleep transistor technique is one of the power gating methodologies which is incorporated into the double latched multiplexed DETFF, for further power reduction. The sleep transistor technique dramatically reduces the leakage power during the circuit in sleep mode [11]. This structure is constructed by totally 20 numbers of transistors with 8 numbers of clocked transistors including inverts I1 and multiplexer.

The NMOS sleep transistors SN1 and SN2 are connected between GND and latch stages (L1, L2) respectively. The PMOS sleep bar transistors SP1 and SP2 are connected between VDD and latching stages (L1, L2) respectively. The CLK, CLK BAR signals can be given as SLEEP and SLEEP BAR signal to NMOS sleep and PMOS sleep bar transistors respectively.

When CLK= HIGH (1), in the first latch L1, SLEEP1=1 and SLEEP1BAR=0. Then the sleep transistors SN1 & SP1 are tuned ON. It makes the latch L1 connected in the DETFF circuit and samples the input data D, and results in Q1=D. At the same time in latch L2, the CLKBAR= LOW (0), SLEEP2=0 and SLEEP2BAR=1. It makes the sleep transistors SN2 & SP2 turned OFF. Due to this, the latch L2 is totally isolated from the DETFF circuit.

When CLK=LOW (0), in the second latch L2, CLKBAR=1, SLEEP2=1 and SLEEP2BAR=0, then the sleep transistors SN2 & SP2 are turned ON. It makes the latch L2 is connected in the DETFF and loads the input data D, results Q2=D. At the same time in latch L1, the SLEEP1=0 & SLEEP1BAR=1, makes both the sleep transistors SN1 & SP1 are turned OFF. Now the latch L1 is totally isolated from DETFF circuit. The output QOUT = Q1 at CLK=1 and QOUT = Q2 at CLK=0.

While any one of the logic latching networks L1 & L2 enters into the sleep mode, the sleep mode latch network will be totally isolated from the DETFF circuit by using sleep transistor technique and reduces the leakage power. However, the additional sleep transistors increase the area, delay and may not retain the original state.

## III. RESULTS AND DISCUSSION

The schematic diagram for proposed Power Gated Double Edge Triggered Flip-Flop (PG-STDETFF) using double latch-multiplexed outputs paradigm and sleep transistor technique is shown in Figure 3.1. The functionality of proposed register element PG-STDETFF is verified under different set of input D and CLK arrivals. Four Operations of proposed register element are given below:

Operation (1): Input data D=1, CLK=1, CLKB=0, L1= Connected to the circuit, L2= isolated from the circuit, Q1=1, Q2=0; output QOUT = Q1

Operation (2): Input data D=1, CLK=0, CLKB=1, L1= isolated from the circuit, L2= Connected to the circuit, Q1=0, Q2=1; output QOUT = Q2

Operation (3): Input data D=0, CLK=1, CLKB=0, L1= Connected to the circuit, L2= isolated from the circuit, Q1=0, Q2=0; output QOUT = Q1

Operation (4): Input data D=0, CLK=0, CLKB=1, L1= isolated from the circuit, L2= Connected to the circuit, Q1=0, Q2=0; output QOUT = Q2

The functionality of proposed register element DMO-PGDETFF is checked under different set of input D and CLK signals. Operation (1) is shown in Figure 3.2. Operation (2) is shown in Figure 3.3. Operation (3) is shown in Figure 3.4. Operation (4) is shown in Figure 3.5. Output waveform of proposed DMO-PGDETFF with Power consumption is shown in Figure 3.6 and its physical layout is exposed in Figure 3.7.

The traditional design optimization metrics to minimize both power and delay of the electronic circuit designs is power delay product PDP. It is referred as energy metric, can be expressed as PDP(energy) = Power (P) × Delay (D). It gives balanced geometric weights to power and delay. PDP optimizes both power and delay equally.

EDP is a supportive metric for evaluating the quality of the design .It is expressed as EDP= Energy × Delay; EDP=P×D×D, But it may not be fit when the low power dissipation is priority. Because EDP gives a top geometric weight to delay than power. This metric is more suitable when the performance is the major concern [21].

PDP gives equal precedence to both power and delay. EDP gives more precedence to delay than power. If power is the higher priority then, both EDP and

PDP matrices may not provide better solutions. For that the new metric power energy product PEP is considered .It gives greater geometric weight to power than delay and produces lower power solution than the other two matrices. It is expressed as PEP = Power × Energy; PEP = P×P×D [22].

The performance parameters such as total number of transistors , number of clocked transistors, Layout area (A), power consumption (P), Delay (D-Q), and optimization metrices such as Power Delay Product (PDP), Energy delay product (EDP), Power energy product (PEP) are taken to evaluate the importance and prospective of the proposed flip flop designs with the existing designs.

Table 3.1 and Table3.2 shows the performance parameters results and the optimization metrices results of existing register elements respectively.

Table 3.3 shows the performance parameters results and Table3.4 shows the optimization metrices results of proposed design respectively. For a better comparison, the bar charts are presented for the performance parameters such as, Number of transistors in Figure 3.8, Number of clocked loads in Figure 3.9, Layout area in Figure 3.10, Delay in Figure 3.11, Power consumption in Figure 3.12, and for optimization metrices such as PDP in Figure 3.13, EDP in Figure 3.14, and PEP in Figure 3.15.

By comparing, the performance parameters results Table 3.1 of existing register elements and performance parameters results table 3.3 of proposed DMO-PGDETFF design, In view of total number of transistors, the proposed design uses totally 20 numbers of transistors with 8 clocked loads. This is minimum number of transistors count compared to existing register elements in Table 3.1 except DDFF design, The proposed design has considerable transistors counts compared to existing DDFF design. DMO-PGDETFF design has same total number of transistors count compared to HLFF design. DMO-PGDETFF achieves 4.76% to 33.33% of total numbers of transistors reduction compared with existing flip-flops in Table 3.1 except DDFF design and 20% to 50% of clocked transistors reduction compared with HLFF and SPGFF register elements respectively. Reduction of total and clocked transistors leads to overall power reduction.

**Table 3.1 Performance Parameters Comparison of Register Elements**

| Register Elements | Performance parameters | | | | | |
|---|---|---|---|---|---|---|
| | Total No. of Transistors | No. of clocked transistors | Triggering mode | Area (μ m2) | D -Q Delay (ps) | Total Power (μw) |
| SPGFF [12] | 30 | 16 | Double | 546 | 162 | 16.4 |
| POWER PC [13] | 22 | 8 | Single | 429 | 176 | 13.424 |
| HLFF [14] | 20 | 10 | Single | 312 | 158 | 12.276 |
| XCFF [15] | 21 | 4 | Single | 338 | 163 | 11.123 |
| SDFF [16] | 23 | 7 | Single | 264 | 156 | 11.028 |
| CDMFF [17] | 22 | 7 | Single | 429 | 178 | 10.277 |
| DDFF [18] | 18 | 6 | Single | 299 | 166 | 9.725 |
| CTS-DETFF [19] | 23 | 8 | Double | 424 | 179 | 8.347 |
| DDNET-D2 [20] | 14 | 2 | Double | 176 | 91 | 7.610 |
| Proposed DMO-PGDETFF | 20 | 8 | Double | 533 | 102 | 50265 |

**Table3.2 Optimization Metrices Comparison of flip-flops**

| Register Elements | Optimization metricies | | |
|---|---|---|---|
| | PDP (fj) | EDP (×10-24) | PEP (×10-20) |
| SPGFF | 2.656 | 0.430 | 4.355 |
| POWER PC | 2.362 | 0.415 | 3.170 |
| HLFF | 1.939 | 0.306 | 2.380 |
| XCFF | 1.813 | 0.295 | 1.135 |
| SDFF | 1.720 | 0.268 | 1.896 |
| CDMFF | 1.829 | 0.325 | 1.879 |
| DDFF | 1.614 | 0.267 | 1.131 |

| | | | |
|---|---|---|---|
| CTS-DETFF | 1.503 | 0.2690 | 1.263 |
| DDNET-D2 | 0.692 | 0.0630 | 0.527 |
| Proposed DMO-PGDETFF | 0.537 | 0.0547 | 0.283 |

Consider the floating node problem the latches L1 and L2 in proposed PG-STDETFF design have no floating nodes because of the separated outputs (X, Y) from the first stage of the latches. This resolves the floating node problem effectively in this proposed design.

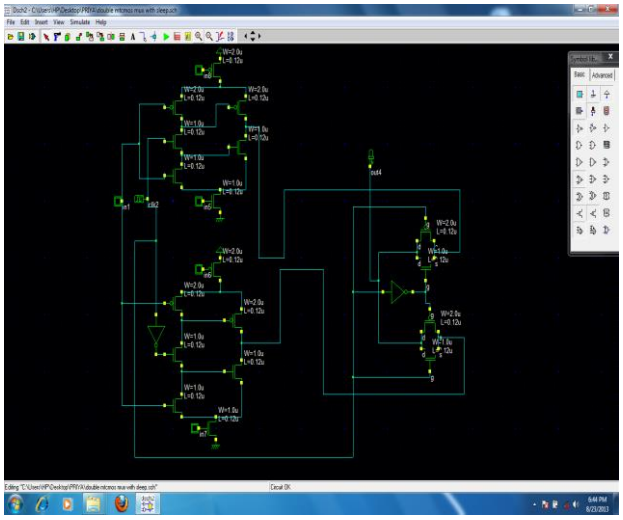

**Figure 3.1 Schematic diagram of proposed PG-STDETFF**

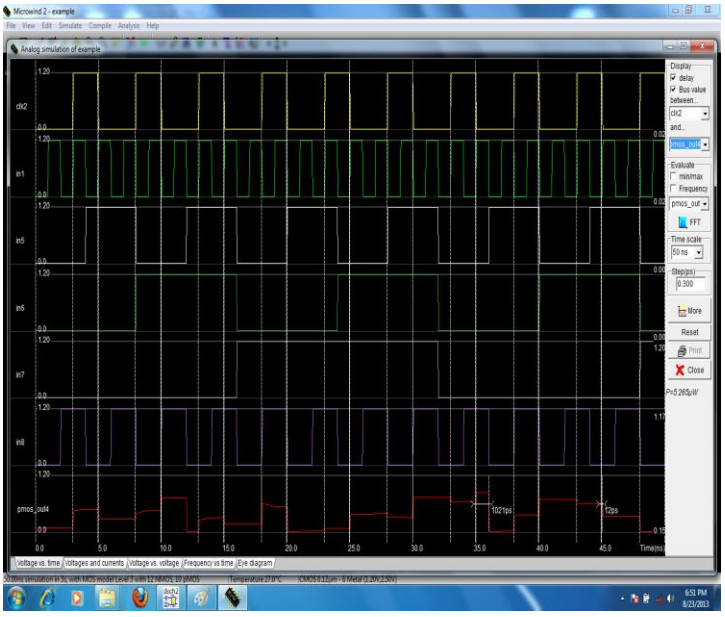

**Figure 3.6 Output waveform of proposed PG-STDETFF (Power consumption = 5.265µw)**

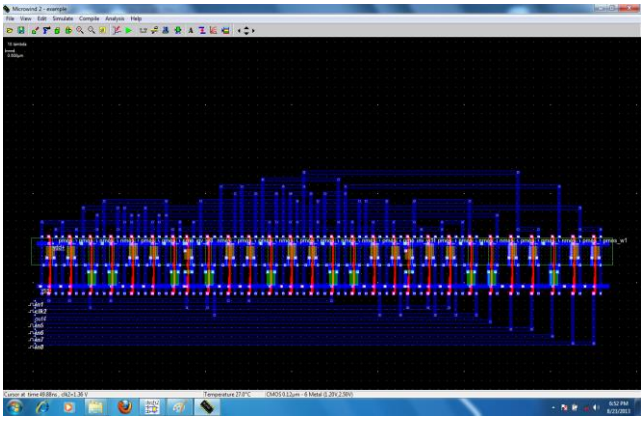

**Figure 3.7 Physical Layout of proposed PG-STDETFF (area= 533µm2)**

The proposed DMO-PGDETFF has the area of 533µm2. Compared with existing SPGFF, the proposed design occupies 2.38% of less area. This design has a considerable area occupation compared with existing flip-flops in Table 3.1,

In view of D-Q delay, the proposed design has the delay of 102ps. This delay value is very minimum compared to existing register elements. In terms of total power consumption, the proposed DMO-PGDETFF consumes the total power of 5.265µw. This proposed design achieves 30.81% to 67.89% of power reduction compared to all existing register elements given in Table 3.1, this low power consumption is achieved mainly due to power gating sleep transistor technique and double latch-multiplexed outputs paradigm.

The proposed DMO-PGDETFF has the PDP value of 0.537 fj. It is improved from 44.40% to 79.78%, compared to all existing flip-flops shown in Table 3.2. The metric PEP gives greater geometric weight to power than delay and produces lower power solution than the other two matrices PDP, EDP. In point of PEP, the proposed design has the value of 0.283×10-20 and improved 61.49% to 93.50% compared to existing flip-flops. It shows that the proposed DMO-PGDETFF design is more suitable for low power clocking systems design.

In view of EDP, it gives a top geometric weight to delay than power. This metric is more suitable when the performance is the major concern. The proposed design has the EDP value of 0.0547×10-24. 56.09% to 87.27% of EDP is improved compared to the existing register elements design. It seems that the proposed design may suitable for high performance clocking systems design also.

## IV. CONCLUSION

In this work a new low power DMO-PGDETFF is proposed for low power clocking system. This register element is designed by the following approaches such as double latch-multiplexed outputs paradigm, dual edge clocking and power gating sleep transistor technique. The proposed design eliminates the floating node problem. A comparison of the proposed register element with the conventional flip-flops showed that it exhibits lower power dissipation along with considerable speed performances.

The post-layout simulation results showed an improvement in PDP by about 44.40% to 79.78%, EDP by about 56.09% to 87.27% compared to the conventional flip-flops. The proposed design has the PEP value of 0.283×10-20 and improved 61.49% to 93.50% compared to conventional flip-flops. It shows that due to minimum power consumption, speed this proposed DMO-PGDETFF circuit may preferable to design the clocking systems where the power dissipation is a major concern with tolerable area overhead.

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